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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/014,407	12/14/2001	Minoru Suzuki	011622	9744

23850 7590 05/22/2003

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EXAMINER	
SOWARD, IDA M	
ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 05/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/014,407	SUZUKI ET AL.	
	Examiner	Art Unit	
	Ida M Soward	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *27 February 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

This Office Action is in response to the Applicants' amendment filed February 27, 2003.

Drawings

The objection to the drawings as failing to comply with 37 CFR 1.84(p)(5) has been withdrawn due to the amendment filed.

Specification

The objection to the title has been withdrawn due to the amendment filed.

Claim Objections

The objection to claims 3 and 5 has been withdrawn due to the amendment filed.

Claim Rejections - 35 USC § 112

The rejection of claim 1 under 35 U.S.C. 112, second paragraph, has been withdrawn due to the amendment filed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2 and 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Webb et al. (5,516,705).

Webb et al. teaches a semiconductor device having, when one of either an N-type or P-type is defined as a first conductivity type, and the other is provided as a second conductivity type, a semiconductor substrate of the first conductivity type, the semiconductor device comprising: first and second buried layers **140** & **160** provided within the semiconductor substrate, being of the first conductivity type, and being of a higher concentration than the semiconductor substrate; first and second emitter layers **132 & 156** of the first conductivity type; first and second base layers **134 & 138** of the second conductivity type, the first and second emitter layers being at least partially embedded within the first and second base layers, respectively; and a portion of the substrate layer **136** is sandwiched between the first and second buried layers, wherein the first and second base layers are positioned on one side surface and the other side surface of the semiconductor substrate so as to form PN planar junctions with the first and second buried layers, the PN planar junctions extending along the first and second base layers and the first and second buried layers, wherein the first and second emitter layers are located in a vicinity of a surface of the inside of the first and second base layers so as to form PN junctions with the first and second base layers, wherein at least a part of the first and second base layers **130** & **154** are respectively provided between the first and second emitter layers and the first and second buried layers, and wherein

at least a part of the first and second buried layers are located between the first and second base layers and the substrate layer. Webb et al. further teach a first metal film **128** formed on one side of the semiconductor substrate and a second metal film **150** formed on the other side of the semiconductor substrate, and the first emitter layer and the first base layer being electrically short-circuited by the first metal film, and the second emitter layer and the second base layer being electrically short-circuited by the second metal film (Figure 5, col. 9, lines 1-65). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the buried layers of Webb et al. to reduce the overshoot voltage value substantially while providing a more sensitive and accurate solid state overvoltage protection device.

Claims 3, 6, 10 and 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Webb et al. (5,516,705) as applied to claims 1-2 and 7-9 above, and further in view of Takizawa (5,962,878) and Assour et al. (4,292,646).

Webb et al. teach all mentioned in the rejection above. However, Webb et al. fail to teach ring-shaped moats. Takizawa teaches first and second moats **16** with bottom surfaces reaching the buried layers formed on both sides of the semiconductor substrate and reaching positions deeper than the bottom surfaces of the base layers, wherein the first and second emitter layers are located inside of the first and second moats; at least a part of the first and second buried layers positioned at a region on the outside of the first and second moats of the surfaces of the semiconductor substrate; and a step of forming moats including the first and second emitter layers inside of the

moats on both sides of the semiconductor substrate (Figure 1). Assour et al. teach a ring-shaped moat **69** (Figure 2, col. 4, lines 9-15). Since Webb et al., Takizawa and Assour et al. are from the same field of endeavor (overvoltage protection devices), the purpose disclosed by Assour et al. would have been recognized in the pertinent art of Webb et al. and Takizawa. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the overvoltage protection device of Webb et al. by incorporating the first & second moats of Takizawa and the ring-shaped moat of Assour et al. to provide lateral isolation from the adjacent region (col. 4, lines 13-15).

Claims 4, 11 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Webb et al. (5,516,705), Takizawa (5,962,878) and Assour et al. (4,292,646) as applied to claims 1-3, 6-10 and 12-14 above, and further in view of Planey (3,772,577).

Webb et al., Takizawa and Assour et al. teach all mentioned in the rejection above. However, Webb et al., Takizawa and Assour et al. fail to teach moats filled with oxide. Planey teaches moats **12** filed with oxide (Figure 3 col. 2, lines 30-51). Since Webb et al., Takizawa, Assour et al. and Planey are from the same field of endeavor (BJT devices), the purpose disclosed by Planey would have been recognized in the pertinent art of Webb et al., Takizawa and Assour et al. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the overvoltage protection device of Webb et al., the first & second moats of

Takizawa and the ring-shaped moat of Assour et al. by incorporating the oxide filled moats of Planey to increase reliability (col. 1, lines 6-11).

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Webb et al. (5,516,705), Takizawa (5,962,878) and Assour et al. (4,292,646) as applied to claims 1-3, 6-10 and 12-14 above, and further in view of Casey et al. (US 6,448,589 B1).

Webb et al., Takizawa and Assour et al. teach all mentioned in the rejection above. However, Webb et al., Takizawa and Assour et al. fail to teach at least part of the base layers positioned at a region on the outside of the moats of the surface of the semiconductor substrate. Casey et al. teach at least part of the base layers **48** & **49** positioned at a region on the outside of the moats **76** & **79** of the surface of the semiconductor substrate **42** & **66** (Figure 2, col. 4-6, all lines). Since Webb et al., Takizawa, Assour et al. and Casey et al. are from the same field of endeavor (BJT devices), the purpose disclosed by Casey et al. would have been recognized in the pertinent art of Webb et al., Takizawa and Assour et al. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the overvoltage protection device of Webb et al., the first & second moats of Takizawa and the ring-shaped moat of Assour et al. by incorporating the base layers of Casey et al. to provide passivation and electrical isolation to the junctions (col. 6, lines 30-32).

Response to Arguments

Applicant's arguments with respect to claims 1-15 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respects to surge protection devices:

Casey et al. (6,531,717 B1) Clark et al. (5,281,832)

Terasawa et al. (4,223,328).

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M Soward whose telephone number is 703-305-3308. The examiner can normally be reached on Monday - Thursday, 6:30 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 703-308-4905. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ims
May 15, 2003

Stephen D. Meier
Primary Examiner